WHAT IS CLAIMED IS:

1. A data transfer system comprising:

a plurality of bus devices, at least one bus device being a bus data supplying device capable of supplying data, at least one bus device being a bus data receiving device capable of receiving data and at least one bus device being a bus master device capable of requesting and controlling data transfer;

a data bus connected to each of said plurality of bus devices and capable of transferring data from a bus data supplying device to a bus data receiving device under control of a bus master device;

a direct memory access unit connected to said data bus as a bus master device, said direct memory access unit including

a source word size register storing a source word size, and

a target word size register storing a target word size,

said direct memory access unit capable of transferring data from a first bus data supplying device to a first bus data recalling device via said first bus by recalling data from a first bus data supplying device in a data size corresponding to said source word data size and supplying said recalled data to a first bus data receiving device in a data size corresponding to said target word size.

2. The data transfer system of claim 1, wherein:

said direct memory access unit further includes

a read data register loaded with data from said bus data supplying device via said data bus in said source word size,

a write data register supplying data to said bus data receiving device via said data bus in said target word size, and

a word formatter connected to transfer data from said read data register to said write data register thereby aligning data in said target word size in said write data register.

3. The data transfer system of claim 2, further comprising:

at least one first bus device being a first bus supplying/receiving device capable of both supplying data to said first bus and receiving data from said first bus.

4. The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer.

5. The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a direct memory access unit which is further capable of controlling data transfer.

6. The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer.

7. The data transfer system of claim 3, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit for loading data into said source data size register and into said target data size register.

8. The data transfer system of claim 3, wherein:

said direct memory access unit further includes

a source start address register storing a source start address,

a source increment size register storing a source increment size,

a target start address register storing a target start address,

a target increment size register storing a target increment size,

said direct memory access unit recalling data from said first bus data supplying device beginning at said source start address and thereafter at successive addresses differing by said source increment size and supplying said recalled data to said first bus data receiving device beginning at said target start address and thereafter at successive addresses differing by said target increment size.

9. The data transfer system of claim 8, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit for loading data into said source start address register, said source increment size register storing, said target start address register and said target increment size register.

10. The data transfer system of claim 3, further comprising:

a bus arbiter connected to each of said at least one bus master device, said direct memory access unit and said first bus, said bus arbiter granting control of data transfer on said data bus to one and only one bus master device; and

said direct memory access unit further includes

a counter value register storing a number of data words to be transferred by said direct memory access unit,

a block size register storing a block size to be transmitted without interruption,

said direct memory access unit requesting bus control from said bus arbiter and upon grant of control of data transmission on said data bus, said direct memory access unit thereafter

transferring data in an amount equal to the lesser of said number of data words to be transferred and said block size to be transmitted without interruption, thereafter

ending data transfer if data transferred equals said number of data words to be transmitted, and

suspending data transfer, releasing control of data transfer on said data bus and re-requesting bus control from said bus arbiter.

11. The data transfer system of claim 10, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit for loading data into said counter value register and said block size register.

12. The data transfer system of claim 1, wherein said plurality of bus devices consist of first bus devices and said data bus consists of a first data bus, said data transfer system further comprising:

a plurality of second bus devices, at least one second bus device being a second bus data supplying device capable of supplying data, at least one second bus device being a second bus data receiving device capable of receiving data and at least one second bus device being a second bus master device capable of requesting and controlling data transfer, each second bus device having a predetermined data size;

a second data bus having said predetermined data size connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device;

a bus bridge connected to said first data bus and said second data bus, said bus bridge capable of transferring data between said first bus devices and said second bus devices; and

wherein said direct memory access unit stores said predetermined data size in said source word size register for data transfer from a second bus device to a first bus device via said bus bridge and stores said predetermined data size in said target word size register for data transfer from a first bus device to a second bus device via said bus bridge.